Claims

What is claimed is:

1. A method, comprising:

allocating a link from a plurality of memory locations included in a memory segment of a memory to a port at substantially a first time, wherein each of the plurality of memory locations includes a plurality of bits.

2. The method of claim 1, further comprising:

partitioning an information array into at least two segments including the memory segment.

3. The method of claim 1, further comprising:

operating the memory segment as a first-in, first-out resource with respect to the port.

4. The method of claim 3, wherein operating the memory segment as a first-in, first-out resource further comprises:

writing a first datum to be enqueued to the port to a first memory location included in the memory segment;

determining an existence of the link; and

writing a second datum to be enqueued to the port to a second memory location included in the memory segment.

5. The method of claim 3, wherein operating the memory segment as a first-in, first-out resource further comprises:

reading a first datum to be enqueued to the port from a first memory location included in the memory segment;

reading a second datum to be enqueued to the port from a second memory location included in the memory segment; and

de-allocating the link.

6. The method of claim 1, further comprising:

allocating a second link from a plurality of memory locations included in a second memory segment of the memory to the port at substantially a second time, wherein each of the plurality of memory locations included in the second memory segment includes a plurality of bits.

7. The method of claim 1, further comprising:

determining a maximum hardware utilization as a number of shareable bits divided by a sum of a total number of information bits and a total number of link bits.

8. An article comprising a machine-accessible medium having associated first data, wherein the first data, when accessed, results in a machine performing:

allocating a link from a first plurality of memory locations included in a first memory segment of a memory to a port at substantially a first time, wherein each of the first plurality of memory locations includes a plurality of bits.

9. The article of claim 8, wherein the first data, when accessed, results in the machine performing:

choosing a number of the first plurality of memory locations by determining a maximum hardware utilization as a number of shareable bits divided by a sum of a total number of information bits and a total number of link bits.

10. The article of claim 8, wherein the first data, when accessed, results in the machine performing:

determining that all of the first plurality of memory locations are occupied by second data; and

allocating a second link from a second plurality of memory locations included in a second memory segment of the memory to the port at substantially a second time, wherein each of the second plurality of memory locations includes a plurality of bits.

11. The article of claim 10, wherein the first data, when accessed, results in the machine performing:

determining that none of the second plurality of memory locations are occupied by second data; and

de-allocating the second link.

12. The article of claim 11, wherein the first data, when accessed, results in the machine performing:

allocating the second link to another port.

13. The article of claim 10, wherein the number of the second plurality of memory locations is the same as the number of the first plurality of memory locations.

14. The article of claim 8, wherein the memory segment is included in a transmit queue storage.

15. An apparatus, comprising:

a port; and

a module to allocate a link from a plurality of memory locations included in a memory segment to the port at substantially one time, wherein each of the plurality of memory locations includes a plurality of bits.

16. The apparatus of claim 15, further comprising:

a memory comprising a plurality of memory segments including the memory segment.

17. The apparatus of claim 16, wherein a number of memory locations in each one of the plurality of memory segments is equal to a number of the plurality of memory locations.

18. The apparatus of claim 15, wherein a number of the plurality of memory locations included in the memory segment is chosen in accordance with a maximum hardware utilization substantially equal to a number of shareable bits divided by a sum of a total number of information bits and a total number of link bits.

19. The apparatus of claim 15, wherein a number of the plurality of bits is equal to an information array width, and wherein the information array width is about equal to or less than the value of $\log_2$ of an information array depth.

20. A system, comprising:

a first port and a second port;

a memory coupled to the first port and to the second port; and

a module to allocate a first link from a plurality of memory locations included in a first memory segment included in the memory to the first port at substantially a first time, and to allocate a second link from a plurality of memory locations included in a second memory segment included in the memory to the second port at substantially a second time, wherein each of the plurality of memory locations included in the first memory segment and the second memory segment includes a plurality of bits.

21. The system of claim 20, further comprising:

an omnidirectional antenna to receive information to be stored in the memory.

22. The system of claim 20, wherein the memory is to store the first link and the second link.

23. The system of claim 20, further comprising:

a communications medium to couple the first port to a data switch.